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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,899	09/23/2003	Akiharu Miyanaga	07977-254003 / US3823D1D1	8644

26171 7590 01/11/2006

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EXAMINER	
VU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,899	MIYANAGA ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *39-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *39-61* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/246014.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.914

1. A request for continued examination under 37 CFR 1.114, including the, fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/14/05 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 39-42, 50-58 are rejected under 35 U. S. C. 102(b) as being anticipated by Sanchez (US Pat. 5,583,067).

Regarding claims 39, 50, 54 and 55, Sanchez discloses in figs. 4f-4g a semiconductor device comprising: a semiconductor substrate (Well); a channel region formed in semiconductor substrate (Well); N+ source /drain regions 52a/52b in channel region wherein channel region is located between N+ source/drain regions 52a/52b wherein each of source and drain regions

52a/52b are provided with a titanium silicide layer 53a/53b on a surface thereof (col. 9, lines 9-28); at least first and second pinning regions 42a/42b (P- doped regions) formed in semiconductor substrate (Well) wherein first and second pinning regions 42a/42b are formed in a vicinity of a boundary between channel region and at least one of the source and drain regions 52a/52b; a gate insulating film 32 formed over the channel region; and a gate electrode 51/53c over the channel region with the gate insulating film 32 interposed therebetween, wherein first and second pinning regions 42a/42b are arranged along boundary and are of a conductivity type (P- type) which is opposite to source and drain regions (N+- type) and wherein first and second pinning regions 42a/42b are overlapped by gate electrode 51/53c at least partly.

Regarding claims 40, 51 and 56, Sanchez discloses that the first and second pinning regions 42a/42b contain an impurity at a concentration of about $1x10^{17}$ atoms/cm^3 (col. 7, lines 29-31).

Regarding claims 41, 52 and 57, Sanchez discloses that a width of first and second pinning regions along boundary is approximately equal to the thickness of the sidewall spacers 46a/46b which is about 0.25 μm (2500Å) (col. 7, lines 55-58 and figs. 4c-4d).

Regarding claims 42, 53 and 58, Sanchez discloses that an interval between first and second pinning regions is less than 0.25 μm (col. 4, lines 15-18 and figs. 4f-4g).

3. Claims 39, 43, 50, 54, 59-61 are rejected under 35 U. S. C. 102(b) as being anticipated by Shimizu et al. (US Pat. 5,217,910, herein after Shimizu).

Shimizu discloses in figs. 9F a semiconductor device comprising: a semiconductor substrate 21; a channel region formed in semiconductor substrate 21; p-source/drain regions (p-doped regions) in channel region wherein channel region is located between p-source/drain

regions; at least first and second pinning regions 38 (n+ -doped regions) formed in semiconductor substrate 21 wherein first and second pinning regions 38 are formed in a vicinity of a first boundary between channel region and the p-source region; at least third and fourth pinning regions 31 (n^--doped regions) formed in semiconductor substrate wherein third and fourth pinning regions 31 are formed in a vicinity of a second boundary between channel region and the p-drain region; a gate insulating film formed over the channel region; and a gate electrode 28/29 over the channel region with the gate insulating film interposed therebetween (figs. 9A-B and col. 8, line 64 through col. 9, line 6), wherein first and second pinning regions 38 are arranged along first boundary and third and fourth pinning regions 31 are arranged along second boundary, and a conductivity type of first, second, third and fourth pinning regions (n-type) are opposite to that of source and drain regions (p-type).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 44-49 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Shimizu et al. (US Pat. 5,217,910) in view of Sanchez (US Pat. 5,583,067).

Shimizu discloses a semiconductor device as described above but fails to disclose the concentration of the first, second, third and fourth pinning region is about $1x10^{17}$ to $5x10^{19}$ atoms/cm^3 (claims 44 and 45); the width of first, second, third and fourth pinning regions along boundary is 0.05 to 0.3 μm (claims 46 and 47); the interval between first and second or between third and fourth pinning regions is 0.04 to 0.6 μm (claims 48 and 49). Sanchez discloses that the first and second pinning regions 42a/42b contain an impurity at a concentration of about $1x10^{17}$ atoms/cm^3 (col. 7, lines 29-31); a width of first and second pinning regions along boundary is about 0.25 μm (col. 7, lines 55-58 and figs. 4c-4d) and an interval between first and second pinning regions is less than 0.25 μm (col. 4, lines 15-18 and figs. 4f-4g). It appears that having a specific width/ interval and concentration of the pinning regions as claimed is prima facie obvious due to the fact that one can vary the width/ interval and concentration of the pinning regions in order to achieve a specific MOSFET device. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined process of Shimizu in view of Sanchez by selecting a suitable the width/ interval and concentration, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In

re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). Moreover, as the width/ interval and concentration of the pinning regions does seem to be critical to the invention, it must be shown that any one or all of the listed materials yield an unexpected product or result. In re Margolis 228 USPQ 940 (Fed. Cir. 1986); In re Kirsch 182 USPQ 286 (CCPA 1974); In re Suether 181 USPQ 36 (CCPA 1974); In re Costello 178 USPQ 290 (CCPA 1973); In re Von Schickh 150 USPQ 300 (CCPA 1966); In re Sussman 60 USPQ 538 (CCPA 1944); In re Kaplan 45 USPQ 175 (CCPA 1940).

Response to Arguments

5. Applicant's arguments filed 11/14/05 have been fully considered but they are not persuasive.

In response to Applicant's arguments that Sanchez does not teach the first and second pinning regions, as indicated in the above rejection, figures 4f-4g of Sanchez clearly discloses claim features (at least first and second pinning regions 42a/42b (P- doped regions) formed in semiconductor substrate (Well) wherein first and second pinning regions 42a/42b are formed in a vicinity of a boundary between channel region and at least one of the source and drain regions 52a/52b).

Applicant's arguments are regarding third and fourth pinning regions. However, as indicated in the above rejection, figure 9f of Sanchez clearly discloses claim features (first and second pinning regions 38 are arranged along first boundary and third and fourth pinning regions

31 are arranged along second boundary, and a conductivity type of first, second, third and fourth pinning regions (n-type) are opposite to that of source and drain regions (p-type)).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (571) 272-1798. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID VU
PRIMARY EXAMINER

January 06, 2006